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| STEP-MAX10 Hardware Manual |
| STEP FPGA |
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| **STEP** |
| **2017/2/14** |

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**STEP-MAX10 Hardware Manual**

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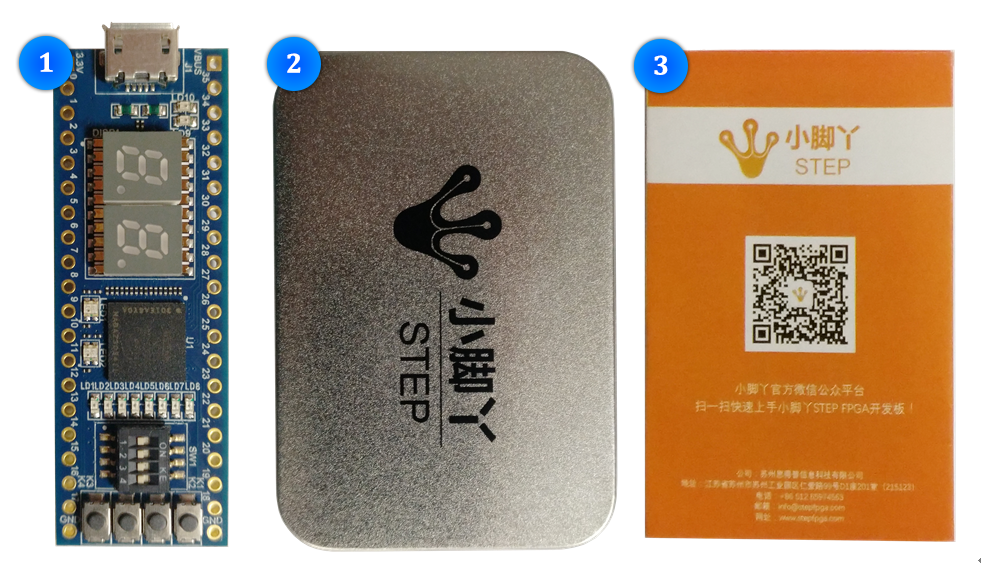
# 1．Introduction

The STEP-MAX10 development board presents a robust, portable and easy-to-learn hardware design platform built around the Altera MAX10 FPGA. The MAX10 FPGA is well equipped to provide cost effective, single-chip solutions in control plane or data path applications and industry-leading programmable logic for ultimate design flexibility. With MAX10 FPGA, you can get lower power consumption / cost and higher performance. If you are a starter to FPGA, the STEP-MAX10 FPGA Development board is your best choice.

The STEP-MAX10 FPGA development board includes hardware such as on-board USB Blaster, 7-Segment Displays, LEDs, GPIOs and much more. By leveraging all of these capabilities, the STEP MAX10 FPGA development board is the perfect solution for learning FPGA, evaluating and prototyping the true potential of the Altera MAX10 FPGA.

# 2．Package Contents

Figure 1 shows a photograph of the STEP-MAX10 package.



**Figure 1 The STEP MAX10 Package contents**

The STEP MAX10 package includes:

1. The STEP MAX10 FPGA Development Board
2. Product Packing Box
3. Quick Start Manual

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| 3．Layout and Components 3.1 Development Board Layout  This section presents the features and design characteristics of the board**.**  A photograph of the board is shown in Figure 2 and Figure 3. It depicts the layout of the board and indicates the location of the connectors and key components.  **Figure 2 Development Board (top view)**  **Figure 3 Development Board (bottom view)**  This board has many features that allow users to implement a wide range of designed circuits, from simple circuits to various creative projects.  3.2 FPGA Device  Now the STEP-MAX10 development board have two version which the only difference of is the FPGA device.   |  |  |  | | --- | --- | --- | | **Version** | **MAX10 10M02** | **MAX10 10M08** | | **Series** | MAX10 | MAX10 | | **Number of LABs/CLBs** | 125 | 500 | | **Number of Logic Elements/Cells** | 2000 | 8000 | | **Total RAM Bits** | 110592 | 387072 | | **Number of I/O** | 112 | 112 | | **Voltage-Supply** | 2.85V-3.465V | 2.85V-3.465V | | **Package/Case** | 153-VFBGA | 153-VFBGA | | **Supplier Device Package** | 153-MBGA(8\*8) | 153-MBGA(8\*8) |   3.3 Programming and Configuration  · On-Board USB Blaster (Normal Micro-USB connector)  3.4 Connecters  · 36 GPIO Header  3.5 Display  · 7-Segment Display ×2  · User LEDs ×8  · RGB LEDs ×2  3.6 Buttons and Switches  · Buttons ×4  · Switches ×4  3.7 Power  · 5V DC input from Micro-USB. 4．Block Diagram of Board Figure 4 gives the block diagram of the board. To provide maximum flexibility for the user, all connections are made through the MAX 10 FPGA device. Thus, the user can configure the FPGA to implement any system design.  **Figure 4 Board Block Diagram** |
| **There are two versions that can be selected: 10M02/10M08** 5．Pins Assignments |

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| **STEP**  **PINs** | **FPGA PINs** | **STEP**  **PINs** | **FPGA PINs** | **Digital**  **Display1** | **FPGA PINs** | **12M**  **CLOCK** | **FPGA PINs** |
| **3.3V** |  | **VBUS** |  | **SEG-A1** | **E1** | **PCLK** | **J5** |
| **GPIO0** | **M4** | **GPIO35** | **B4** | **SEG-B1** | **D2** | **LED** | **FPGA PINs** |
| **GPIO1** | **P3** | **GPIO34** | **A5** | **SEG-C1** | **K2** | **LED1** | **N15** |
| **GPIO2** | **M5** | **GPIO33** | **A7** | **SEG-D1** | **J2** | **LED2** | **N14** |
| **GPIO3** | **R3** | **GPIO32** | **B6** | **SEG-E1** | **G2** | **LED3** | **M14** |
| **GPIO4** | **L6** | **GPIO31** | **E7** | **SEG-F1** | **F5** | **LED4** | **M12** |
| **GPIO5** | **P4** | **GPIO30** | **D7** | **SEG-G1** | **G5** | **LED5** | **L15** |
| **GPIO6** | **L7** | **GPIO29** | **B7** | **SEG-DP1** | **L1** | **LED6** | **K12** |
| **GPIO7** | **R5** | **GPIO28** | **C8** | **SEG-DIG1** | **E2** | **LED7** | **L11** |
| **GPIO8** | **P6** | **GPIO27** | **B8** | **Digital**  **Display2** | **FPGA**  **PINs** | **LED8** | **K11** |
| **GPIO9** | **R7** | **GPIO26** | **D10** | **Switch** | **FPGA PINs** |
| **GPIO10** | **P7** | **GPIO25** | **A9** | **SEG-A2** | **A3** | **SW1** | **J12** |
| **GPIO11** | **P8** | **GPIO24** | **A11** | **SEG-B2** | **A2** | **SW2** | **H11** |
| **GPIO12** | **P9** | **GPIO23** | **A13** | **SEG-C2** | **P2** | **SW3** | **H12** |
| **GPIO13** | **R9** | **GPIO22** | **B11** | **SEG-D2** | **P1** | **SW4** | **H13** |
| **GPIO14** | **R11** | **GPIO21** | **A14** | **SEG-E2** | **N1** | **Button** | **FPGA PINs** |
| **GPIO15** | **P12** | **GPIO20** | **B13** | **SEG-F2** | **C1** | **KEY1** | **J9** |
| **GPIO16** | **R14** | **GPIO19** | **B14** | **SEG-G2** | **C2** | **KEY2** | **K14** |
| **GPIO17** | **P15** | **GPIO18** | **B15** | **SEG-DP2** | **R2** | **KEY3** | **J11** |
| **GND** |  | **GND** |  | **SEG-DIG2** | **B1** | **KEY4** | **J14** |
| **RGB LED1** | **R** | **G** | **B** | **RGB\_LED2** | **R** | **G** | **B** |
| **FPGA PINs** | **G15** | **E15** | **E14** | **FPGA PINs** | **C15** | **C14** | **D12** |

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# 6．Version

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| **Version number** | **Date** | **Comments** |
| 1.0 | 2017/2/14 | Initial Revision |